

# Total Interconnect Solution Provider

Investor Relations 2023

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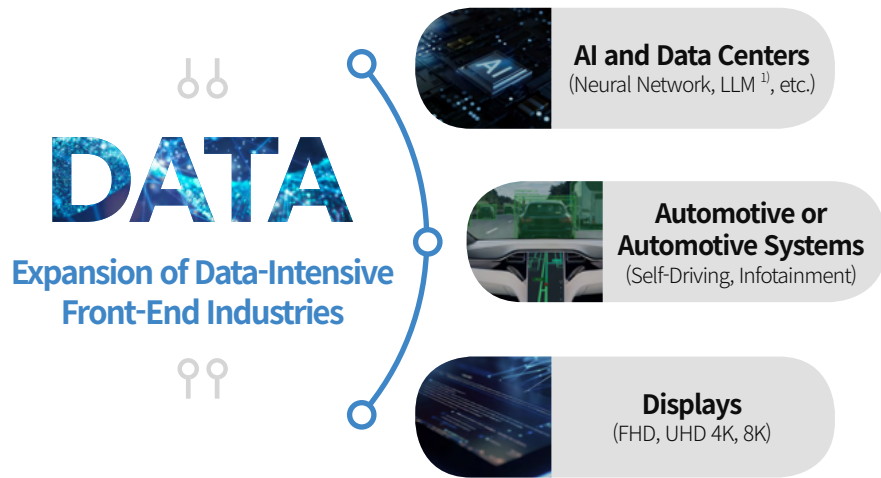


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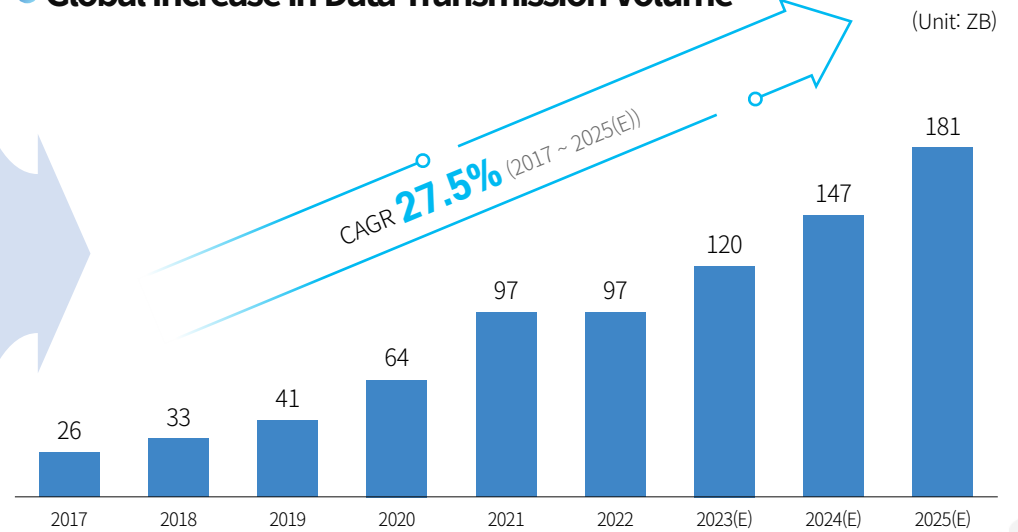
The background features a collage of images: a network diagram with blue nodes and lines, a close-up of a circuit board with a blue component, and abstract blue light trails on a dark background. The collage is overlaid with a grid of squares in white, light blue, and dark blue, some with diagonal lines.



## Increasing data exchange among various devices fueled by Advances in ICT Technology



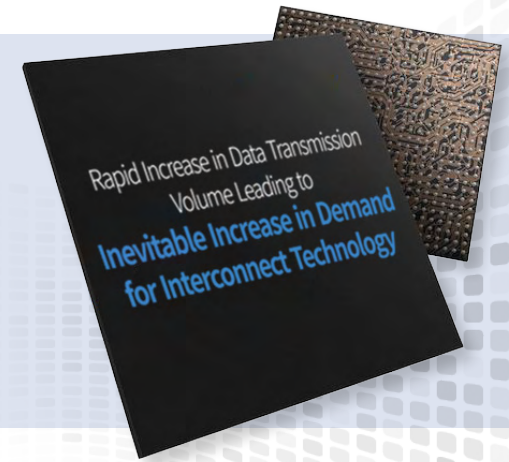
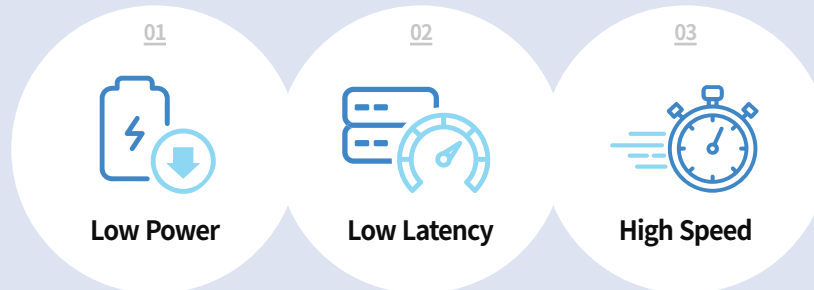
### Global Increase in Data Transmission Volume



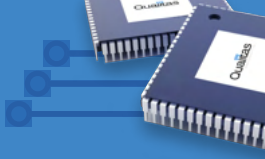
### High-Speed Interconnect Technology?

High-Speed Transmission of Data in Vast Quantities

### [ Key Requirements of High-Speed Interconnect Technology ]

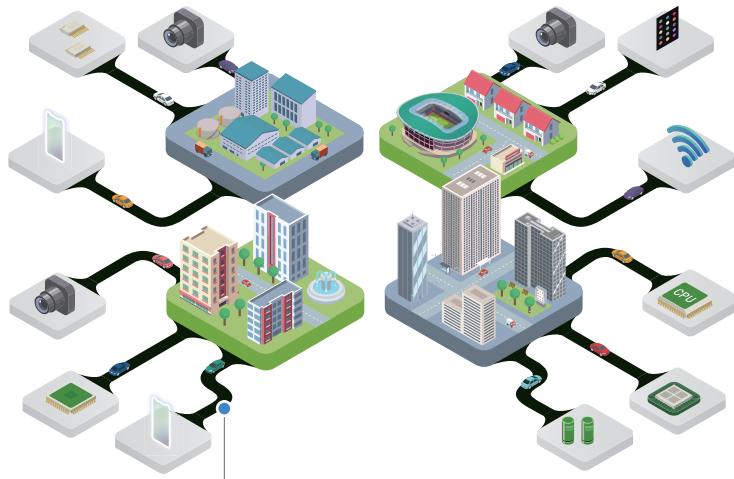


※ 1) LLM: Large Language Model  
※ Source: Statista, Hyundai Motor Securities



## High-Speed Interconnect: An Essential Foundation for All Applications

- : SoC
- : Data
- : Interface IP (Qualitas Semiconductor's Business Segment)
- : External Components (Other SoCs, Camera Display Panels, Memory, etc.)

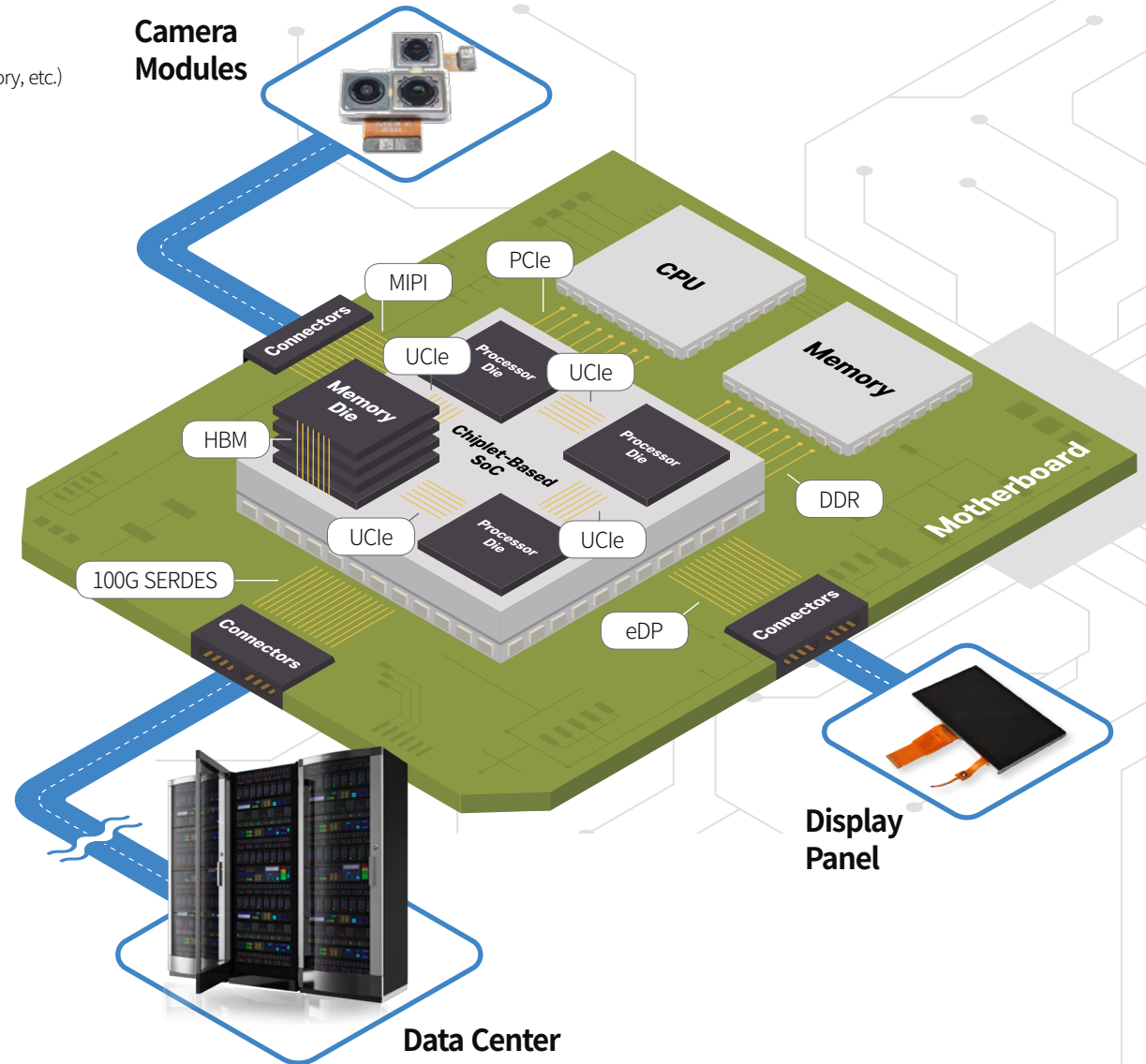
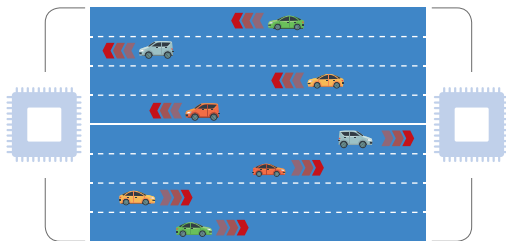


### Concept Map

Existing Solutions



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## The Semiconductor IP Industry reduces Costs and Time on SoC Development

**Increasing Demand for Highly-Reliable IP Vendor**

Sharp Increase in Average SoC Development Costs

65nm ▶ 3nm

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**20x ↑** in Design Costs

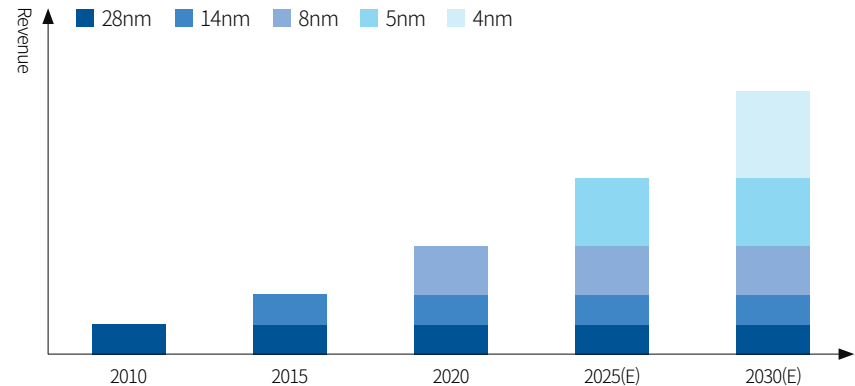
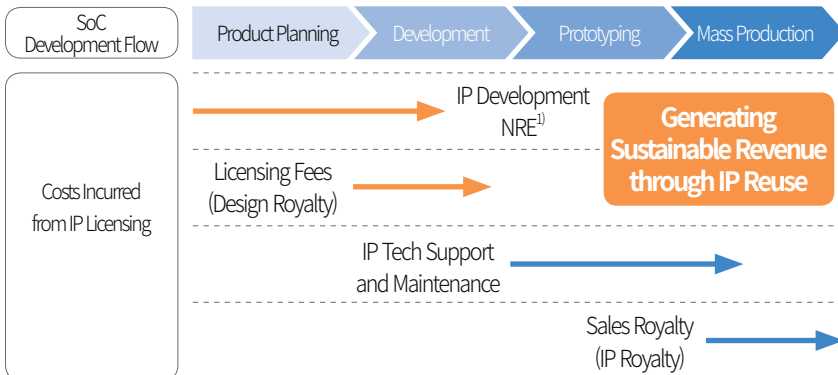
Increase in the Number of IPs Required for SOC Development

2012 ▶ 2016

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**1.5x ↑** in Number of IPs Applied Per SOC

### Revenue Structure Characteristics of the Semiconductor IP Industry



- Design Royalty Leads to Highly-Profitable Recurring Revenues
- Continuous Cash Flow from Licensing Fees at Each SoC Development Stage

**▶ High Revenues & Steady Cash Flow**



- Accumulative Revenue Structure through IP Reuse
- Higher profit is achieved as process nodes are more advanced

**▶ Long-tail Business without Inventory**

※ 1) NRE(Non-Recurring Engineering): Initial Development Costs



### Imbalance between demand and supply

**01 Wider Applications**  
Expanded Applications Enabled by ICT Technology Advancements

**02 Increase in Data Transmission Speeds**  
Higher Transmission Speeds Required by Applications

**03 Growth in ASIC<sup>1)</sup> Demand**  
Expansion of Semiconductor IP Customer Base Due to Higher AI Chip Demand

**Key Growth Drivers of the Semiconductor IP Market**

**01 Small Number of Semiconductor IP Suppliers**  
Verified IP Mass Production Experience

**02 Semiconductor IP Entry Barriers**  
Highly-Skilled Personnel and Steep R&D Costs Required

**03 Design Capability for Advanced Process**  
Absolute Shortage of IP Suppliers  
Capable of Cutting-edge Design Processes



※ 1) ASIC (Application-Specific Integrated Circuit): Customized Semiconductors



## A Rising IP provider in High-end Interconnect Technology, a Key Infrastructure of the Semiconductor Industry



### Technologies Powering Future Industries Including AI, Data Centers, and Self-Driving

#### High-Speed Interface IP Licensing and Design Services

##### High-Speed Interconnect Semiconductor Design Technology

**High-Speed Interconnect Technology Gaining Prominence in the System Semiconductor Industry**

- Growth in the Foundry Industry Fueled by the Increase in SoC Demand Across Many Sectors
- Emergence of Various ICT Technologies Including AI, Mobile, Self-Driving, and Displays

##### Cutting-edge Semiconductor Process Design and Testing Technology

**Established Track Record in the Development and Mass Production of Cutting-Edge Semiconductor Processes**

- Possession of Highly Reliable Design Methodology for Cutting-edge Semiconductor Processes
- Difficulty Level of Cutting-edge FINFET<sup>1)</sup> Process Designs >>> Difficulty Level of Planar CMOS Process<sup>2)</sup> Designs

※ 1) FinFET: Process Designed to Increase Performance and Reduce Leaking Currents to Overcome the Limitations of Traditional 2D Planar Processes

2) Planar CMOS Process: Manufacturing and Connecting Semiconductor Components on Silicon Substrates



# 03 Why Qualitas? ② Early Foundry Ecosystem

Semiconductor IP is Key to Ensure Speed-to-Market for SoCs

Development Cost ↓    Development Time ↓    Mass Production Reliability ↑

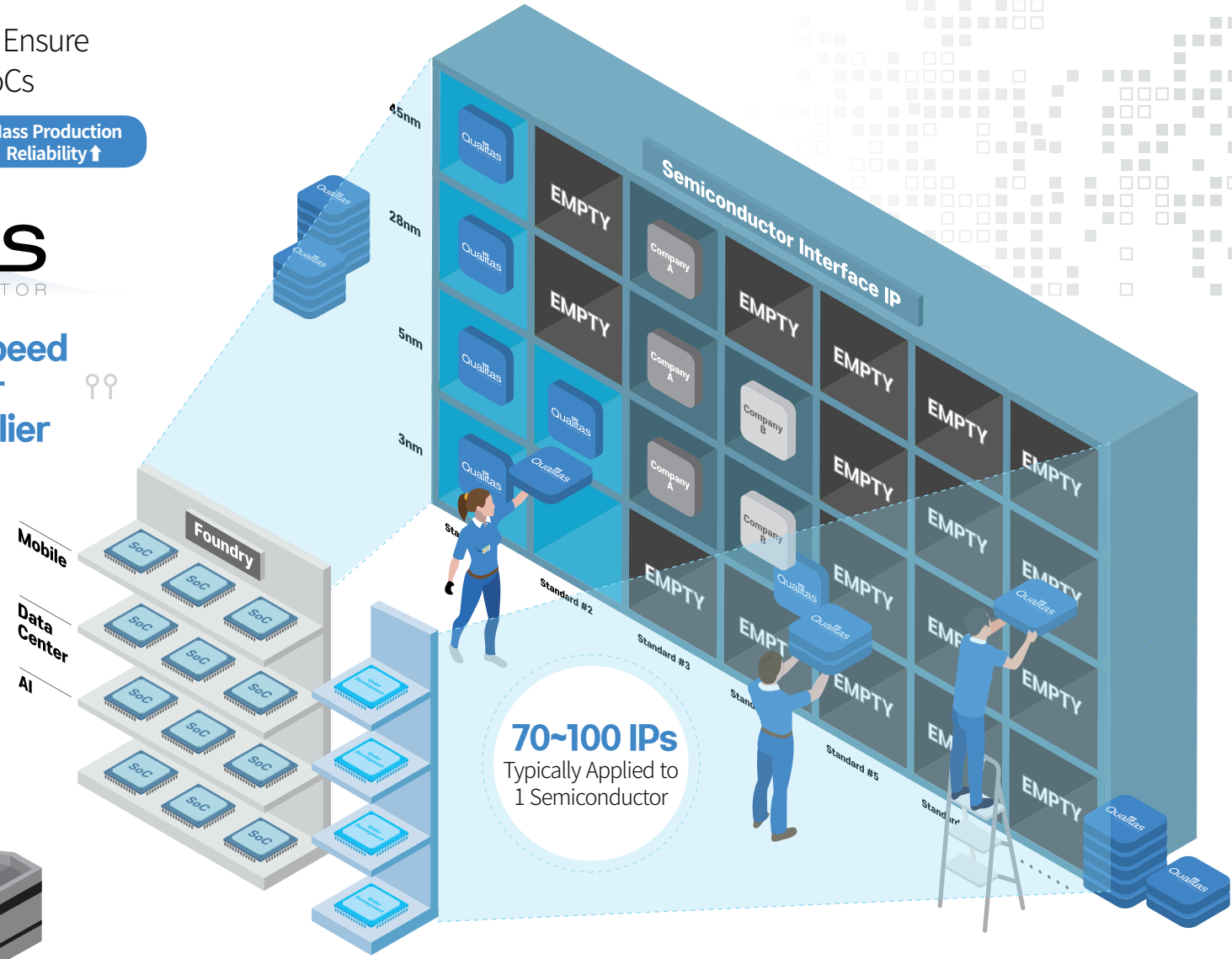


Dominating High-Speed Interface Sector as an ideal IP supplier

"I Would Like a Mobile AP for the 3nm-Process."

SAMSUNG  
tsmc

AMD  
intel  
NVIDIA



## Top-Class Technology

7th Global Firm with 100G SERDES  
Circuit Design Technology

## Global Partnership

Key Interface IP Partner for  
Samsung Foundry

## AA

AA, A Ratings Acquired  
in Technical Evaluations

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## 152 Employees

Korea's Largest IP Vendor  
comprised of 84% R&D Workforce

## 186%

Three-Year CAGR of Revenues  
(2020~2022)

## 52

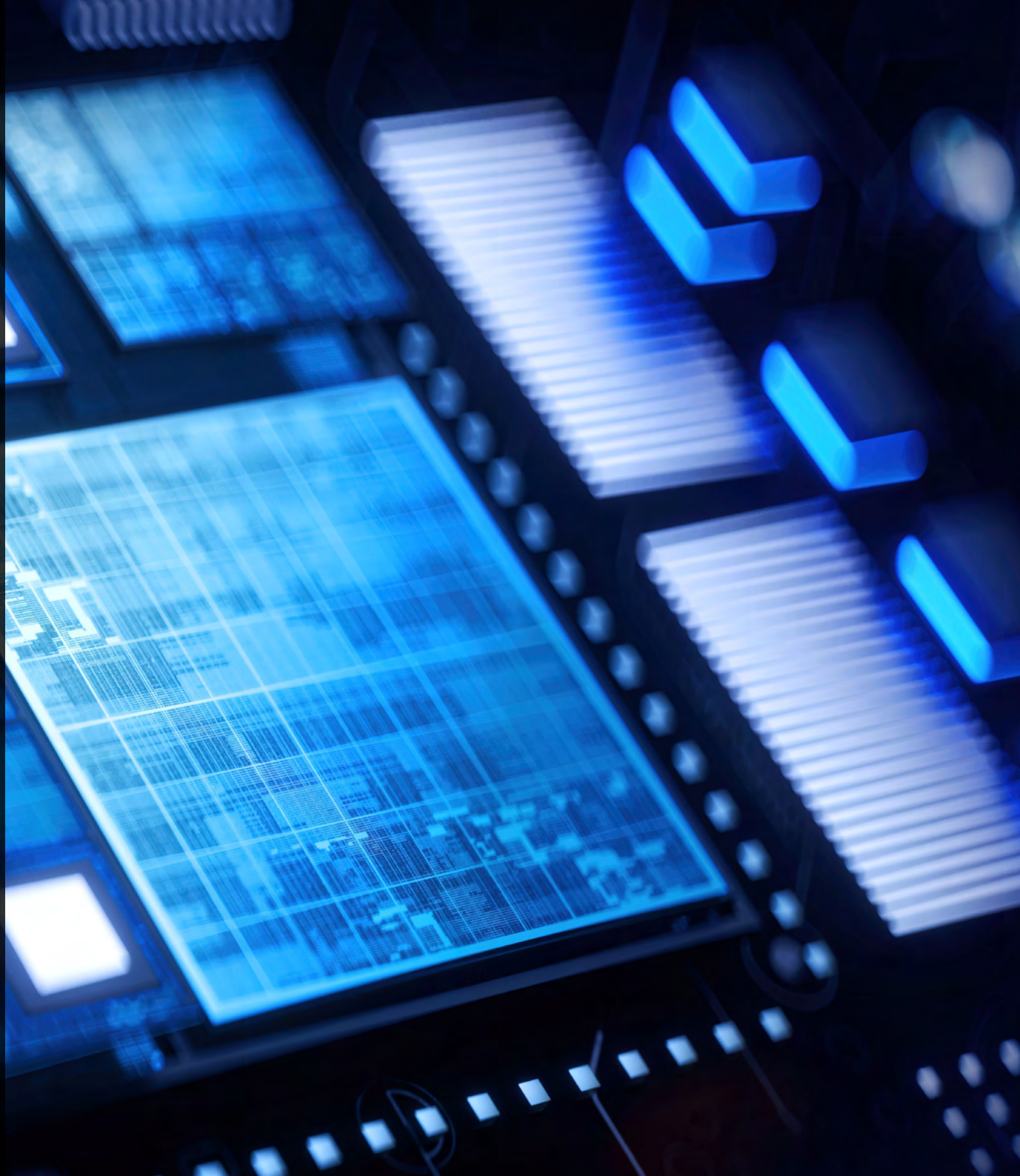
Number of IP Licensing Agreements

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# 01

## Key Corporate Highlights

- 01. Summary
- 02. Largest R&D Workforce in Korea's IP Industry
- 03. Mutual Growth with Key Clients
- 04. World-Class Technical Competitiveness
- 05. Diversification of IP Product Portfolio
- 06. Exponential Growth in the IP Industry



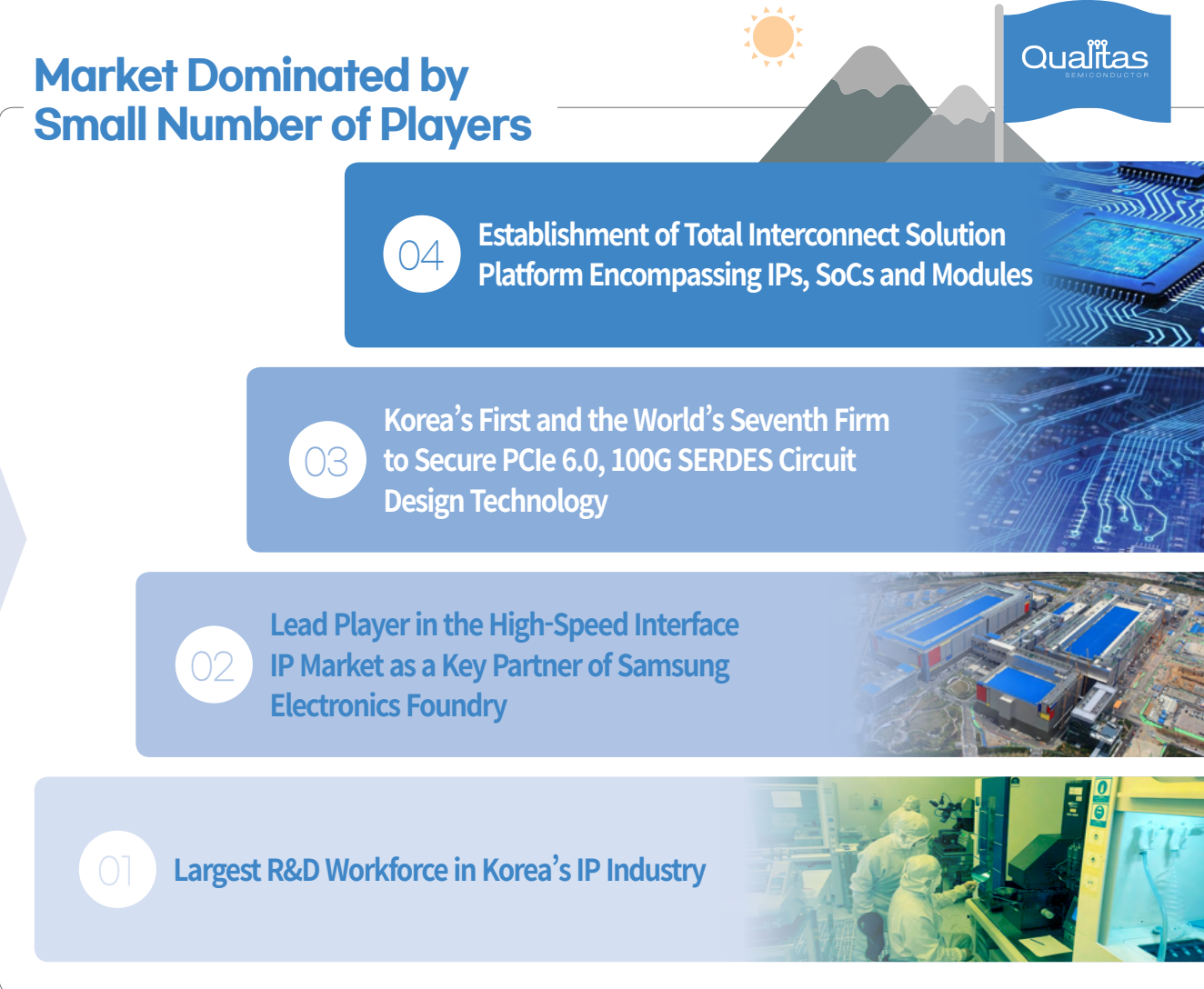


## Unrivaled Position in the Domestic Interface IP Market Due to High Entry Barriers

- Entry Barrier for New Players**
- Proven Track Record of IP Mass Production
  - High-Speed Interconnect Design Technology
  - Cutting-edge Semiconductor Process Design Technology
  - Highly-Skilled Technical Workforce

Entry Barriers

### Market Dominated by Small Number of Players

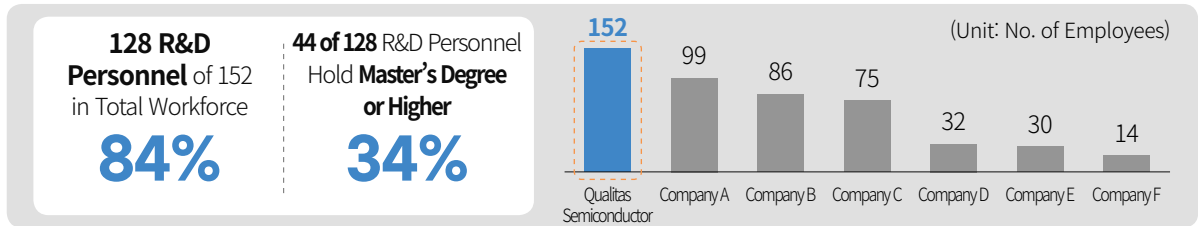


# 02 Largest R&D Workforce in Korea's IP Industry

## Best High-Speed Interface IP Team in Korea

**Duho Kim**  
CEO, Ph.D.

- Yonsei University (Ph.D.)
- Samsung Electronics
- Korea Credit Information Services



**Pyungsu Han**  
Executive Director, CTO, Ph.D.

- Head of Research
- Yonsei University (Ph.D.)
- LG Electronics

**Ilhyun Kyung**  
Managing Director

- Head of Business
- Inha University
- Wellang

**Seunghwan Yu**  
Director, CFO

- Finance Management, Sogang University
- EY Hanyoung
- Hanwha Investment & Securities

**Application Engineering Team**  
**Kwangchun Choi**  
Executive Director Ph.D.

- Yonsei University (Ph.D.)
- Samsung Electronics

**13** Employees

**Optical Interconnect Development Team**  
**Jaeyoung Kim**  
Managing Director, Ph.D.

- Yonsei University (Ph.D.)
- NTT, Rohm

**14** Employees

**SERDES IP Development Team**  
**Chankyung Seong**  
Managing Director, Ph.D.

- Yonsei University (Ph.D.)
- Samsung Electronics

**41** Employees

**Mobile IP Development Team**  
**Cheol Heo**  
Director, M.S.

- Pukyong National University (M.S.)
- DB HiTek, LX Semicon

**23** Employees

**Controller IP Development Team**  
**Jaechul Lee**  
Managing Director, M.S.

- Korea University (M.S.)
- Samsung Electronics, DB HiTek

**14** Employees

**Display IP Development Team**  
**Yonghyun Park**  
Director, M.S.

- Sogang University (M.S.)
- LG Electronics

**22** Employees

※ The number of employees in each company and team is as of August 2023

# 04 World-Class Technical Competitiveness

## Top-Tier Global Position Through the Development of 100G SERDES and PCIe 6.0 PHY



### Secured Key Technologies in Semiconductor IP

Semiconductor Design Technology for High-Speed Interconnect

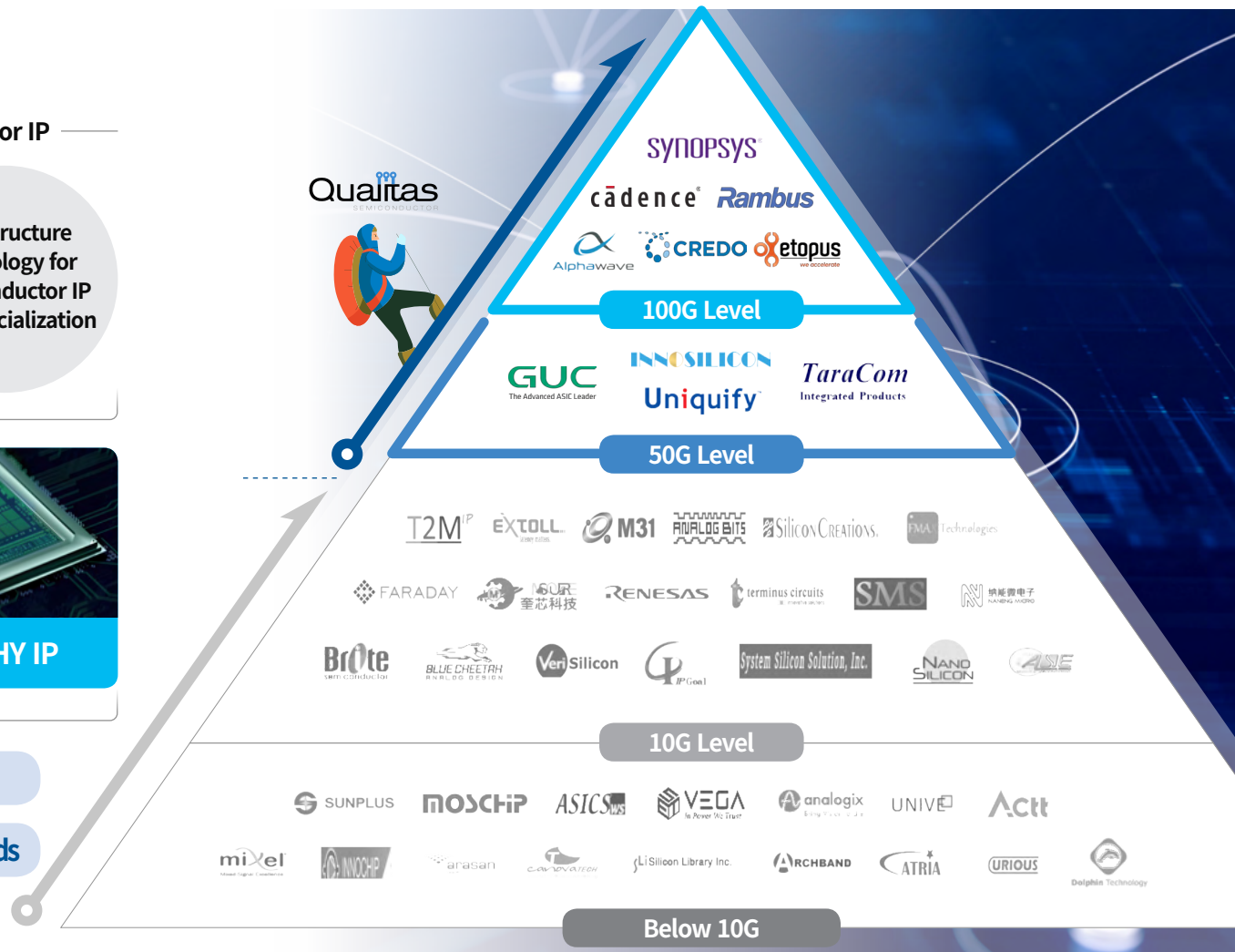
Cutting-edge Semiconductor Process Design and Testing Technology

Infrastructure Technology for Semiconductor IP Commercialization



World's Seventh Developer

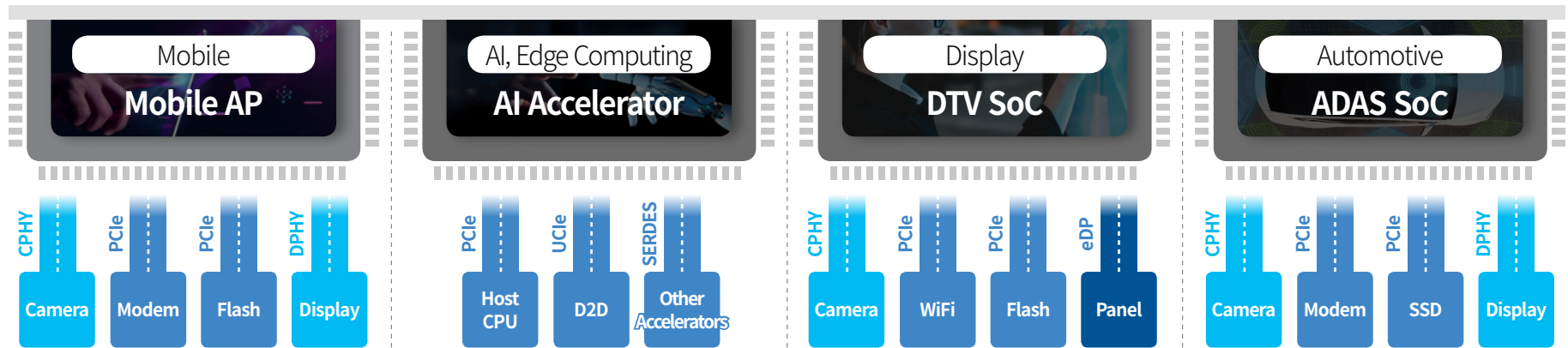
Scalability to Meet Most Existing Standards





## Market Lead and Mass Production Track Record Established in Various High-Speed Interface IP Sectors

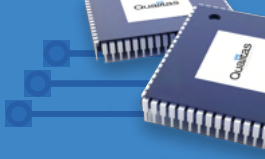
### IPs by Application



### Competitive Advantage in Qualitas Semiconductor IP

| Category              | <b>MIPI</b><br>(Mobile Industry Processor Interface)                       | <b>PCIe / SERDES</b><br>(Peripheral Component Interconnect Express)             | <b>Display Chipset</b>                                          |
|-----------------------|----------------------------------------------------------------------------|---------------------------------------------------------------------------------|-----------------------------------------------------------------|
| IP Type               | D-PHY, C-PHY, Controller                                                   | PCIe 4.0 PHY, SERDES, PCIe 6.0 PHY                                              | eDP RX PHY, eDP TX PHY, Intra panel                             |
| Characteristics       | Increasing Demand for Interface IP in Cutting-edge Semiconductor Processes | Growing Need for Applications in AI, Self-Driving and Other Advanced Industries | Growing Demand for Display Miniaturization Processes            |
| Production Status     | D-PHY, D-PHY / C-PHY Combo PHY                                             | PCIe 4.0 PHY                                                                    | eDP RX PHY, Intra-Panel Interface TX PHY                        |
| Competitive Advantage | <b>Multiple Mass Production Track Record in Samsung Foundry</b>            | <b>The World's Seventh PCIe 6.0 PHY Under Development</b>                       | <b>Strengthened Market Position Through FinFET Process Lead</b> |

# 06 Exponential Growth in the IP Industry

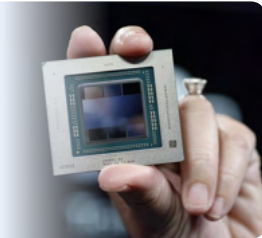


## IP Business Characterized by “3 Highs”

### IP Business Characteristics

#### “High” Demand

Sustained Growth in Demand Due to Limited Availability of Verified IP Vendors



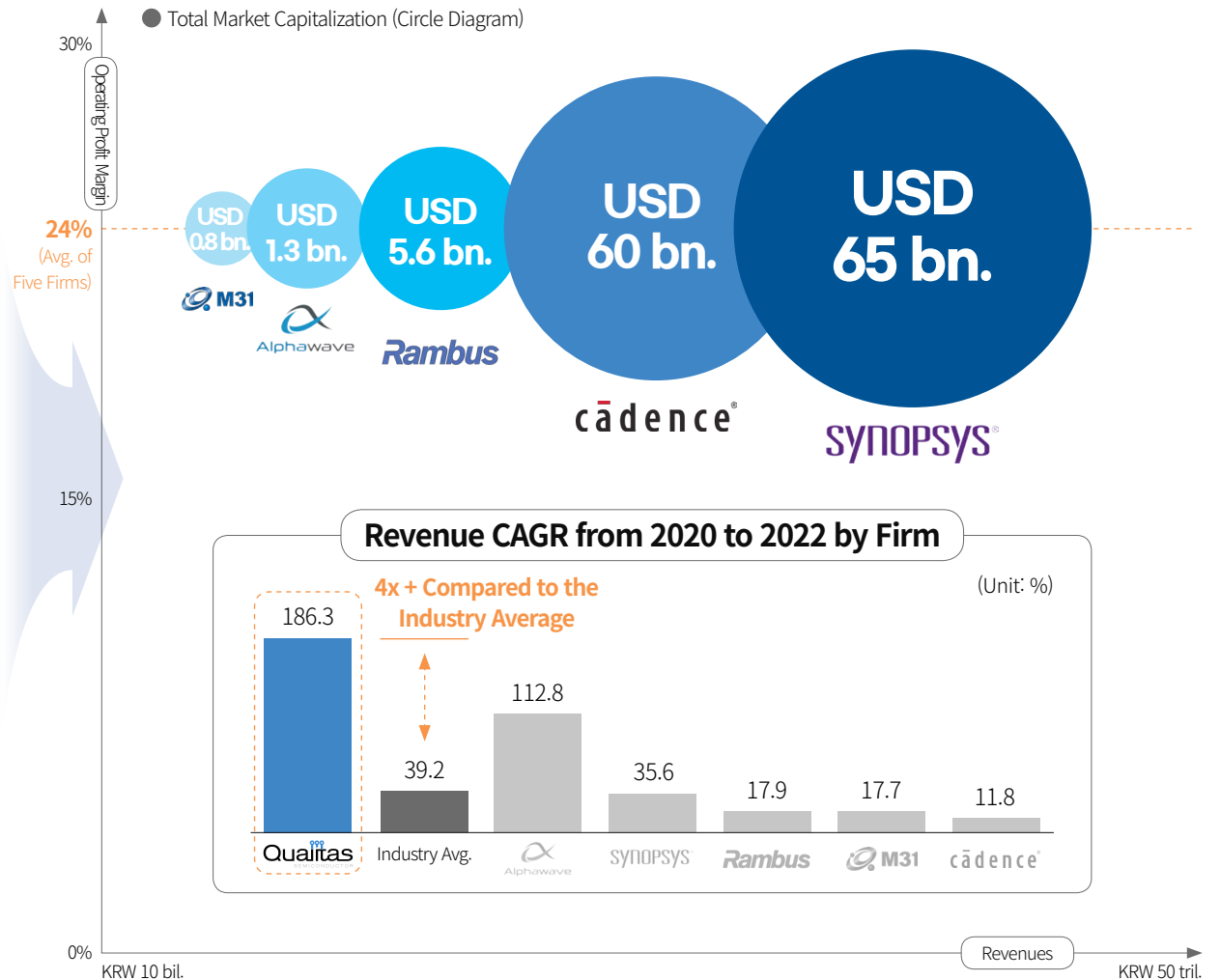
#### “High” Growth

Rapid External Growth Through Reuse After Building an IP Portfolio



#### “High” Profits

High Profitability Structure Enabled by Increasing Demand for Cutting-edge Processes and High Value-Added IP



※ Based on Annual Reports from  
 ※ Total Market Capitalization as of Aug. 17, 2023

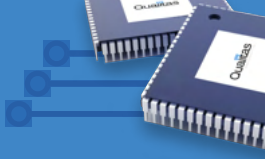


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# 02

## Market Overview

- 01. Expansion of the Global Semiconductor IP Market
- 02. Interface IP: Essential infrastructure in Semiconductor IP



# 01 Expansion of the Global Semiconductor IP Market

## Growth of Downstream Industry + Development of ICT = Simultaneous Growth in Semiconductor IP Quantity and Price

### Factors Increasing Semiconductor IP Price

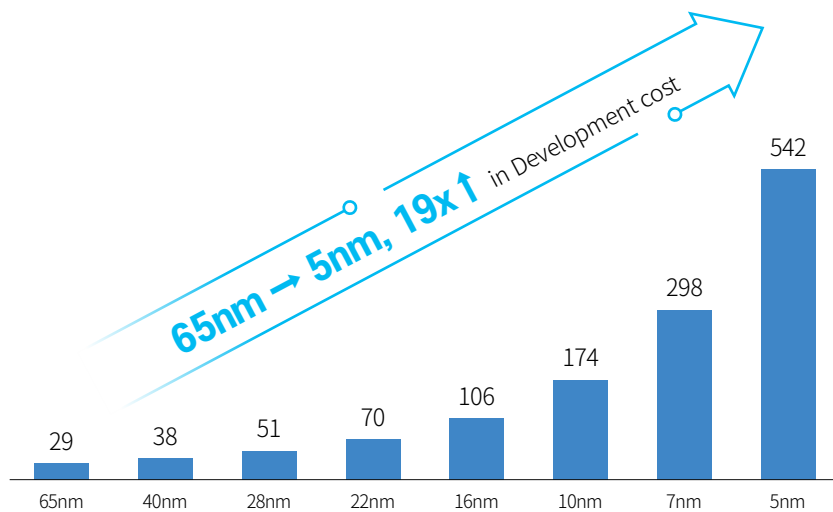


### Factors Increasing Demand for Semiconductor IP



### SoC development cost for semiconductor process

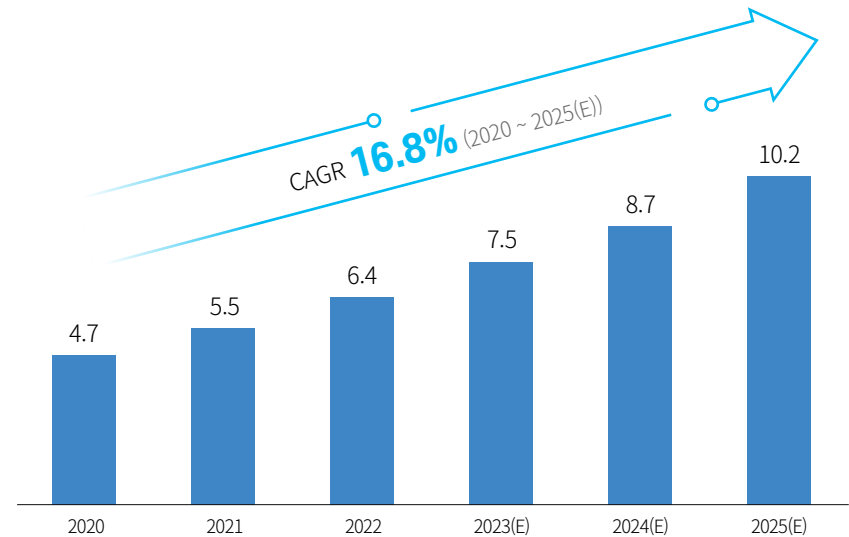
(Unit: \$M)



※ Source: IBS (International business strategies)

### Global Semiconductor IP Market Outlook

(Unit: \$B)

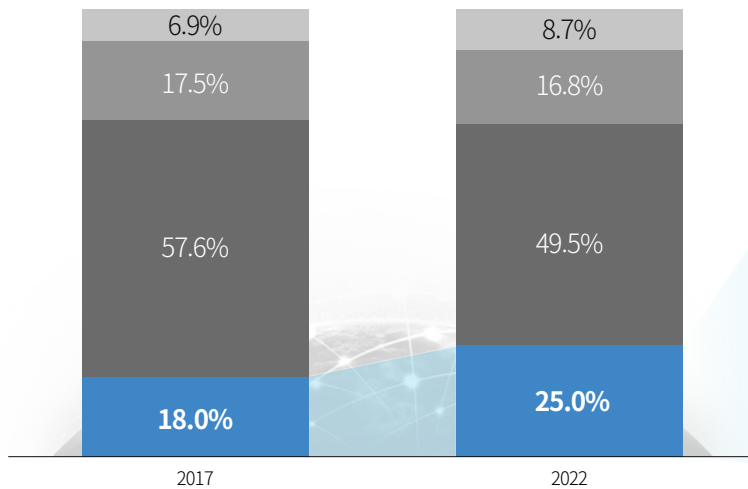


※ Source: IPnest (May 2022), Press Clipping

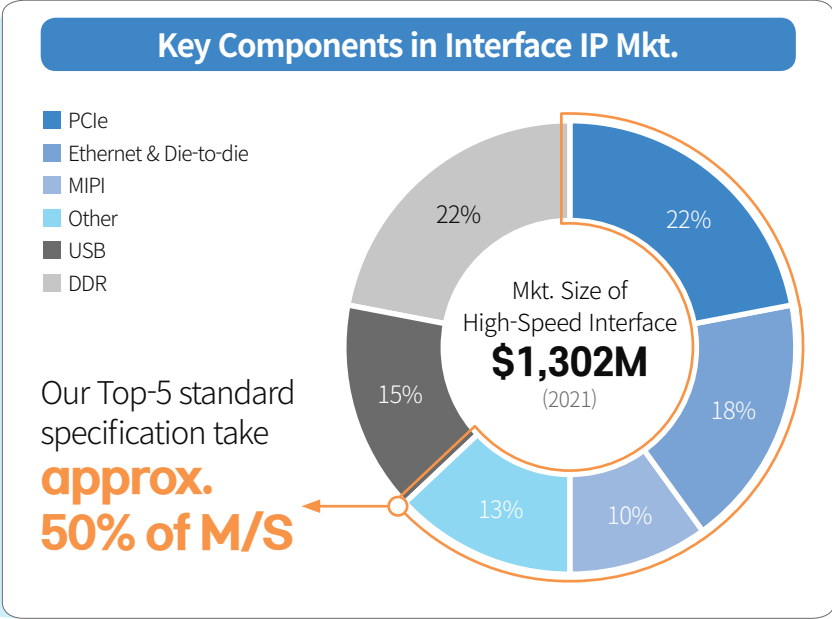
## Favorable Environment as Increased Demand in Interface IPs

### Changes in Global IP's proportion by Year

■ Interface ■ Processor ■ Physical ■ Digital Other



※ Source: Ipnest 2023



### Factors Increasing Demand for Semiconductor IP



#### Advance in Downstream Industry

Increased data processing speed for mobile, AI, and autonomous driving etc.

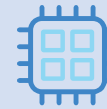
+



#### Maximization of Energy Efficiency

Low energy consumption required for mobile devices and data centers among others

+



#### Advance of the Processing Technology

As chips' integrity level increased, types and units of IPs needed also increased

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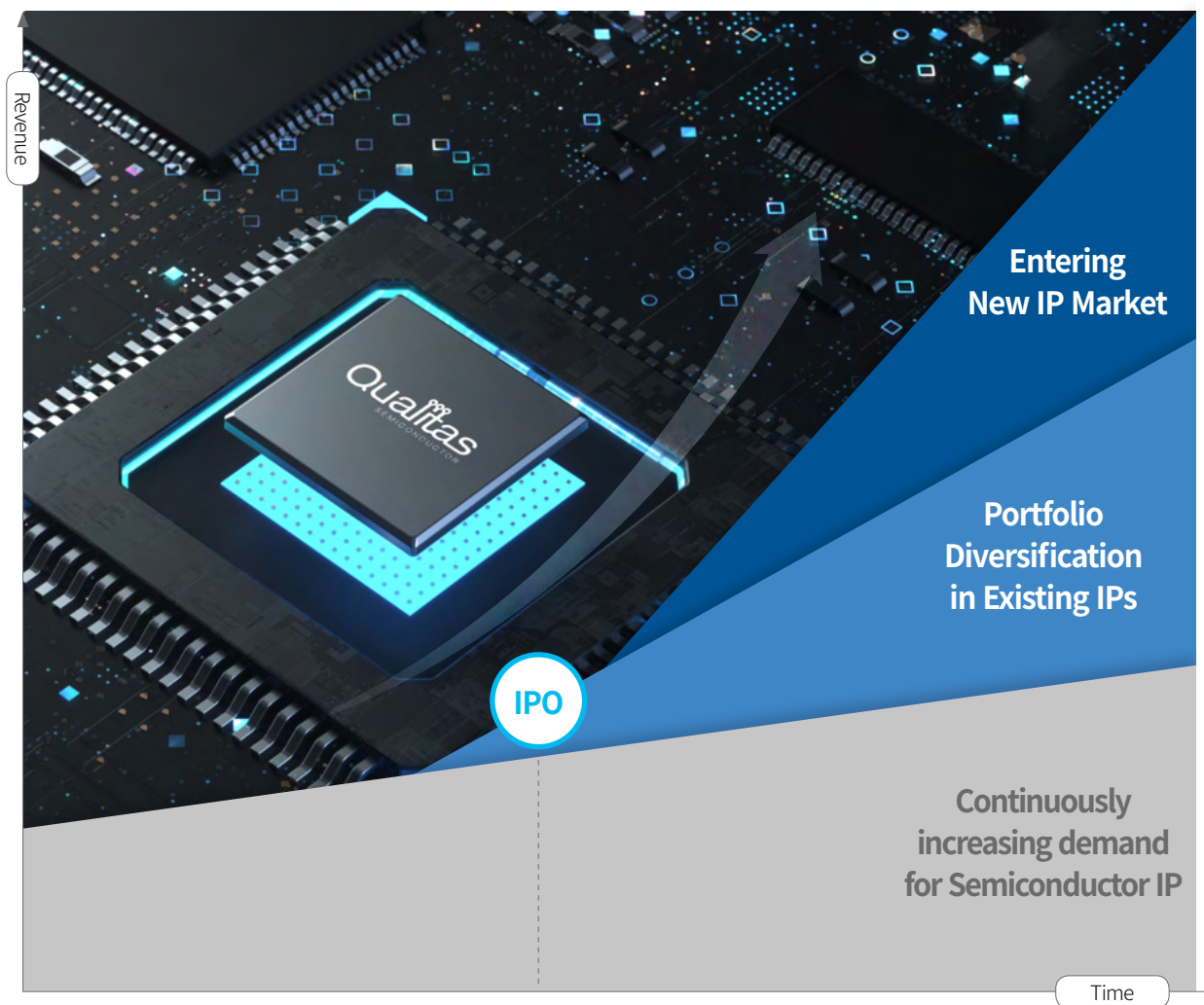
# 03

## Growth Strategy

- 01. Summary
- 02. Expansion of IP Portfolio for High-Speed Interface Solutions
- 03. Entering the High Value-Added IP Market
- 04. Preemptive Strategy Establishment to Secure Customers
- 05. Financial Projection



## Leader in High-Speed Interconnect Technology



### Entering the High Value-added IP Mkt.

- Preemptive development of future-oriented core technologies including UClE and PCIe 6.0
- Providing a total solution for interconnects that combines IP + SoC + modules



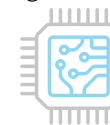
### Strengthening Mkt. Dominance

- Expansion of existing IP processes and implementation of next-generation standards
- Expansion of the scope of customers based on a rich history of mass IP production



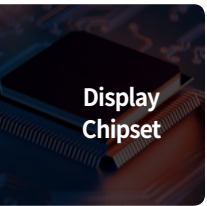
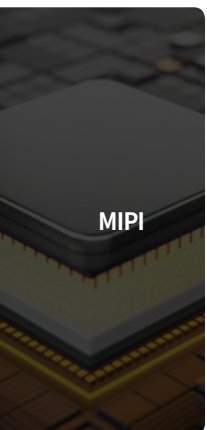
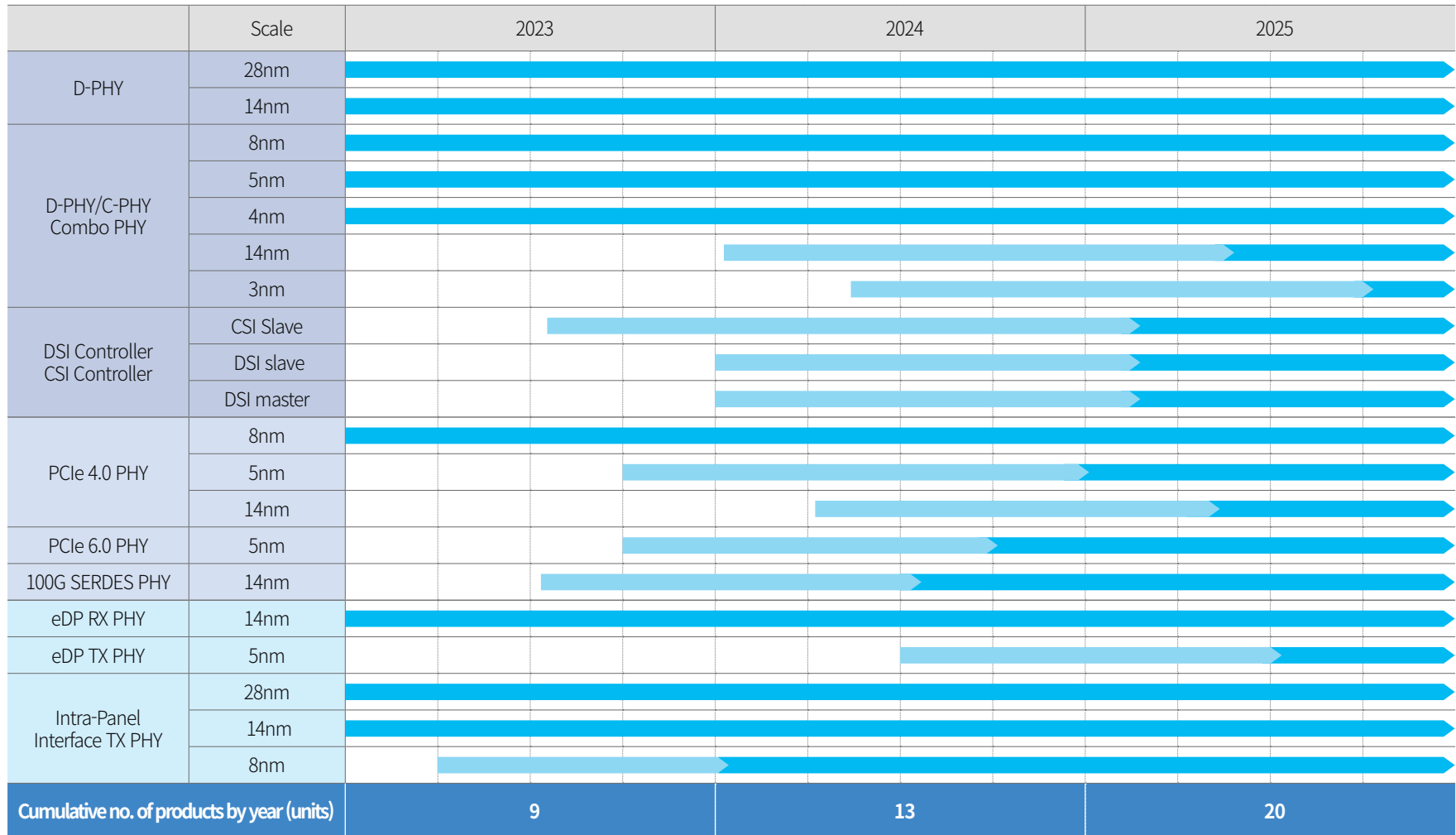
### Growth of System Semiconductor and Foundry Industry

- Exponential increase in demand for Interface IP
- Rising development costs for cutting-edge semiconductor processing



## IP Portfolio Accommodating Advanced Process Nodes & Implementing Next-Generation Standards

Development stage Mass production stage



## Strengthen Competitiveness for Market Dominance by Preemptively Securing Next-Generation IP Products

### PCIe 6.0 PHY IP

- Highly versatile IP used in all fields
- Average contract price: 2x of existing products (PCIe 4.0)

An integration of the cutting-edge interconnect technology



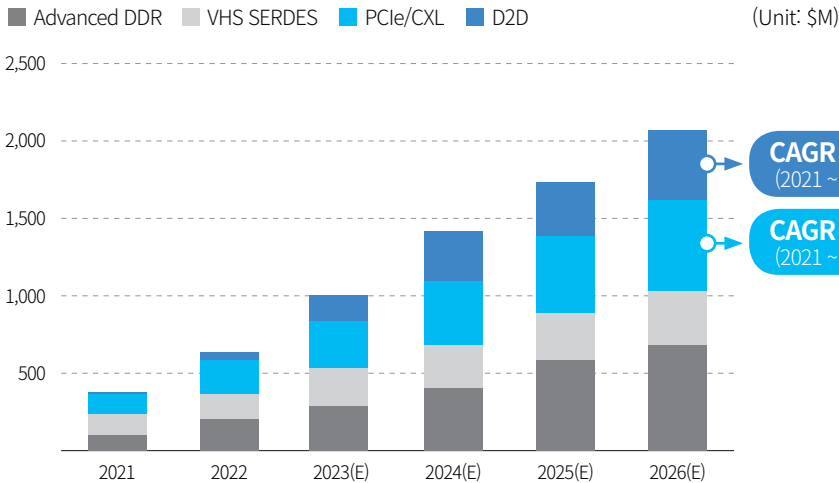
### UCIe PHY IP

- One of the most widely used IP standards along with HBMs
- Super high pricing is projected

Aiming to become the first company to commercialize the tech in Korea



### High-end Interface IP's Mkt. Scale



#### Portfolio Expansion

Expansion to next-generation standard interface specifications

PCIe 6.0

CXL<sup>1)</sup> 3.0

UCIe<sup>2)</sup>

#### Entering various finished goods industries

Core IP for high-tech industries (e.g. AI & auto-driving)

Data Center

Autonomous Driving

AI

#### Securing competitiveness in winning orders

Market dominance based on technological gap

Global top-tier designing capability

Cutting-edge process design and verification

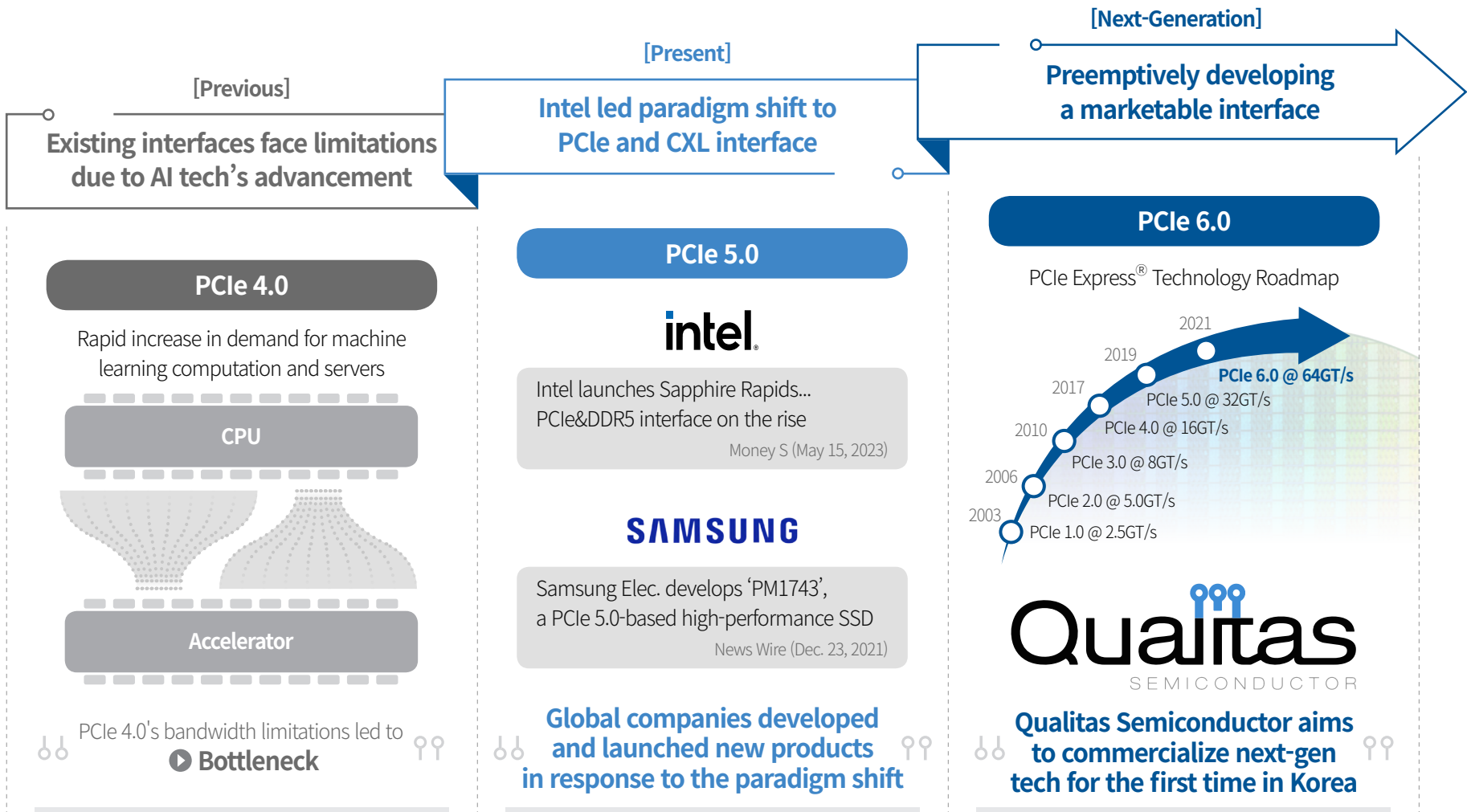
Market Dominance through First Domestic Commercialization

※ Source: "IPnest Forecast Interface IP Category Growth to \$2.5B in 2025", IPnest

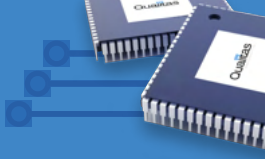
※ 1) CXL: Technology built on the PCIe physical layer, providing low-latency & high-speed interconnect between CPUs and devices, utilizing the PCIe PHY standard

2) UCIe (Universal Chiplet Interconnect Express)

## Qualitas is the Greatest Beneficiary of the Next Generation Interface Overcoming the Limitations of Existing Interfaces







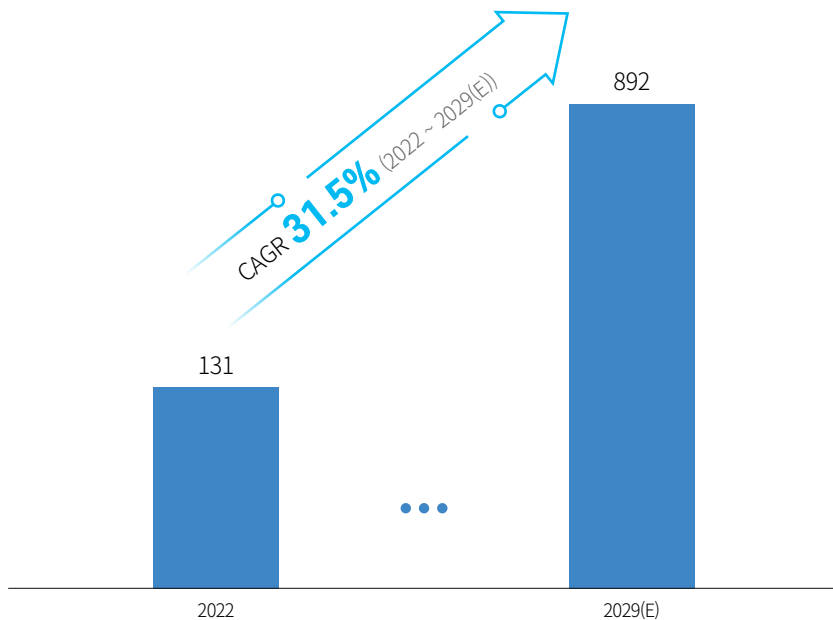
## Dominate the High Value-Added IP Market by Securing Compatibility with the Rapidly Emerging CXL

### ○ CXL Interface IP's Market Size

Samsung Electronics develops “CXL 2.0 DRAM”, a next-generation memory... The first in the industry  
*Money S (May 15, 2023)*

Chat GPT isn't a challenge to us... CXL-based large-scale AI acceleration system has been launched  
*Seoul Economy Daily (Apr. 28, 2023)*

(Unit: \$M)

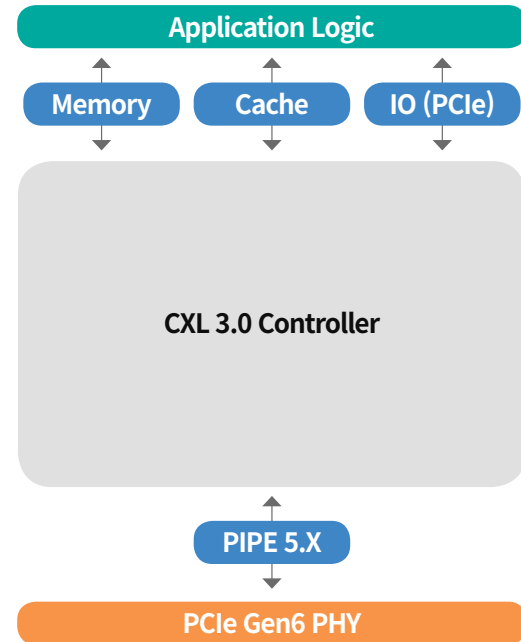


※ Source: Global CXL Controller IP Market Research Report (2023)

### PCIe 6.0 / CXL 3.0's Compatibility

Compatibility with PCIe 6.0-based CXL 3.0 contributes to increased connection speed

<CXL Org. Chart>



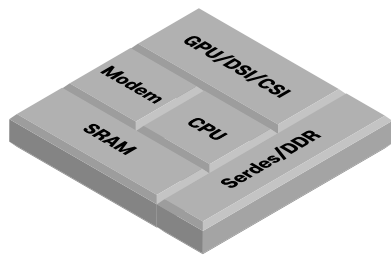
**Aiming to supply PCIe 6.0 PHY,  
the physical layer of CXL**





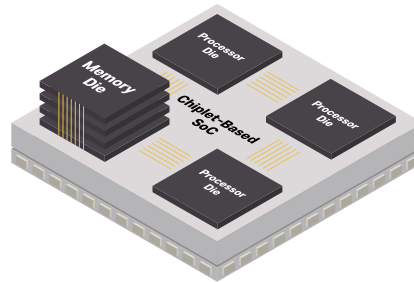
## Increase in Data Transmission + Advance of ICT Technology = Exponential Increase in Chiplet Demand

### Tech Comparison between Monolithic Chips vs. Chiplets



#### [ Monolithic ]

An SoC consolidating all functions onto a single die



#### [ Chiplet ]

An SoC with high-performance features divided across multiple dies and packaged together

### Strengths of Chiplets



**Reduces SoC development costs and risks**

Multiple dies can be integrated directly into a single package using the most suitable process



**Reduces R&D time**

Increased productivity by reusing existing chiplets



**Increase in Net Dies**

Increased production unit per wafer by reducing chip area

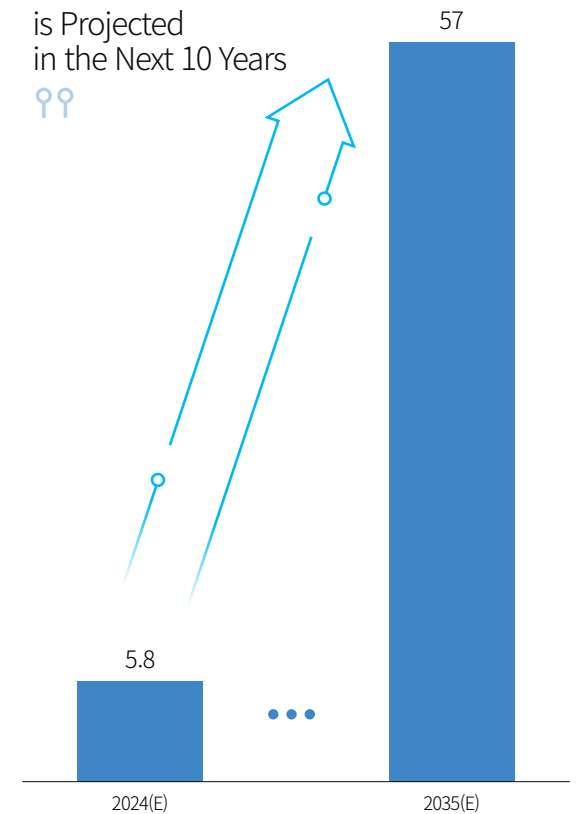
### Chiplet's market size by year

(Unit: \$B)



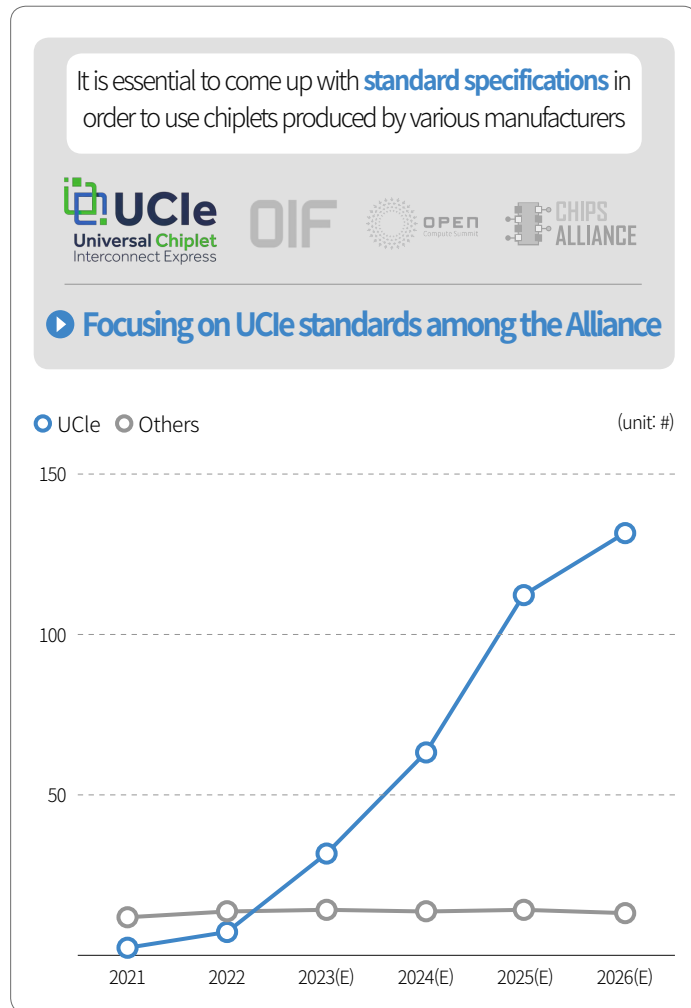
#### 10x Growth

is Projected in the Next 10 Years

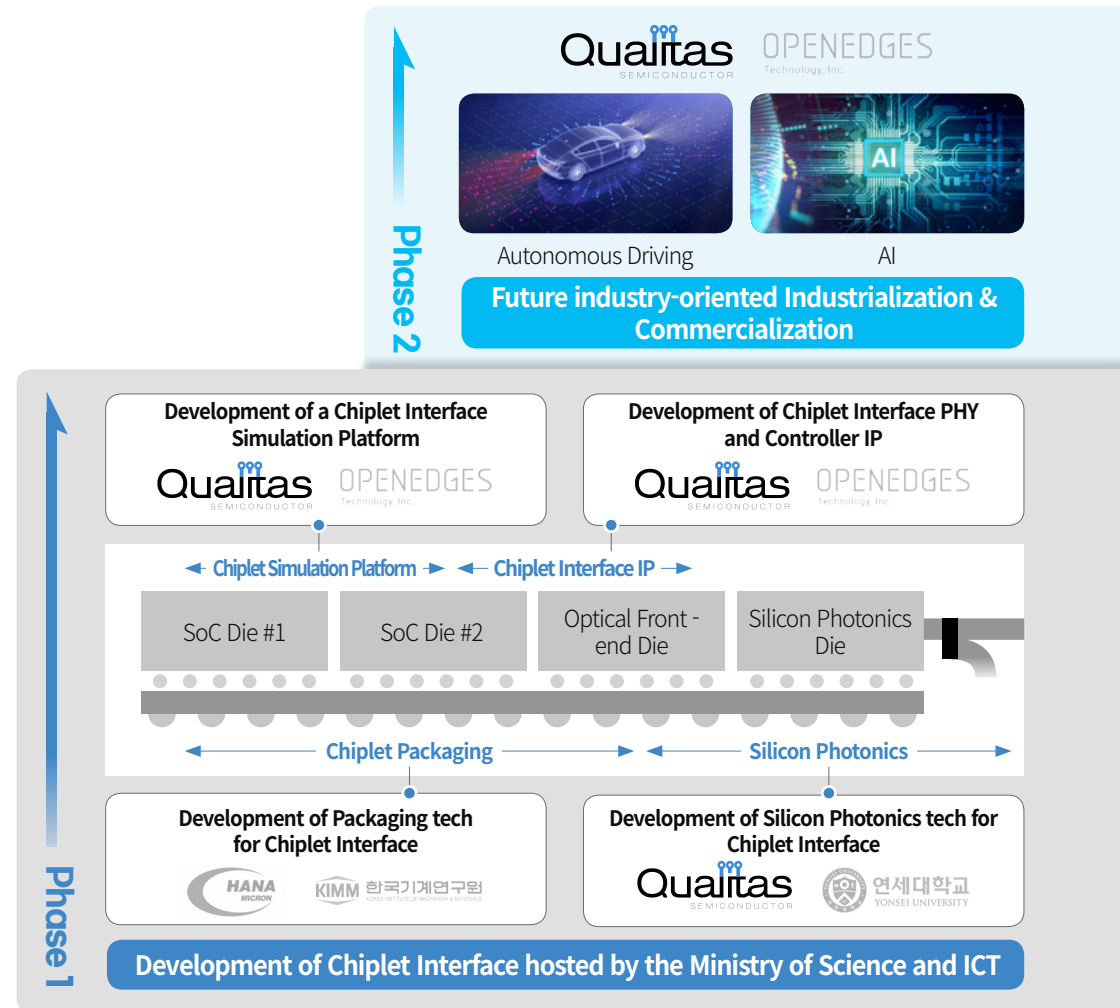


※ Source: Omdia

## Dominating the Market by Preemptively Developing Marketable Technology



※ Source: SemiWiki



## Strengthen marketing capabilities for increasing end-customers in all area



### Customer-base expansion plan



**Securing customers**  
through foundry companies with high reputation



**Direct technology interaction**  
with SoC manufacturers



**Foundry Diversification Strategy**